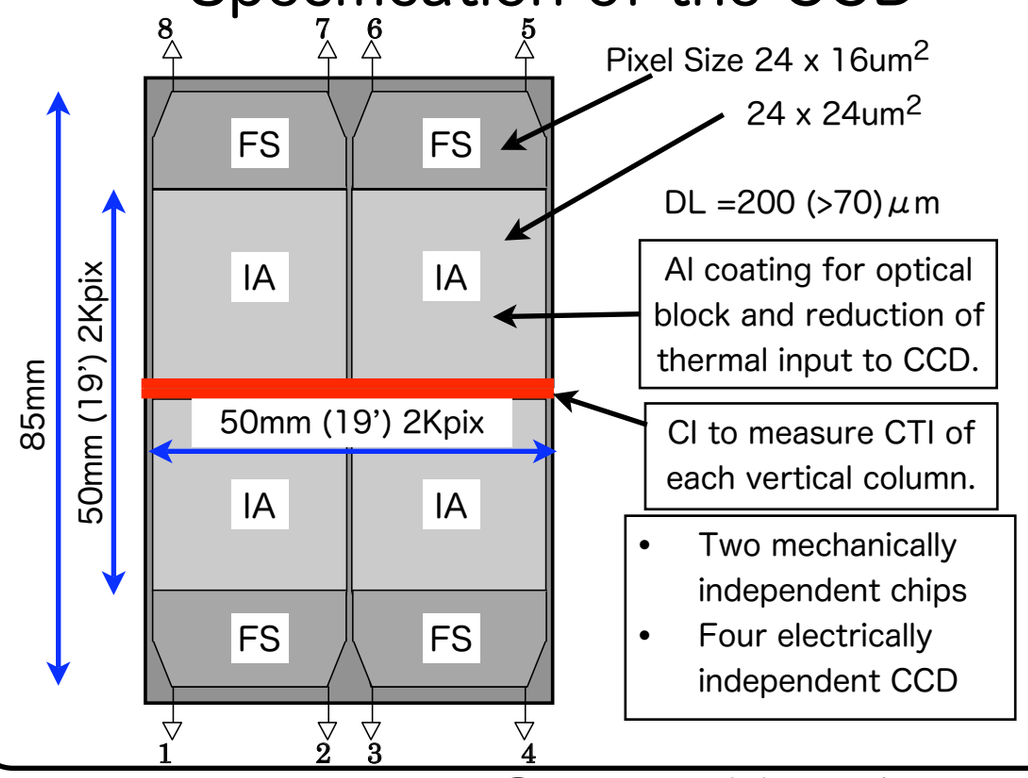
Soft X-ray Imager (SXI) onboard the NeXT satellite

The NeXT/SXI Team

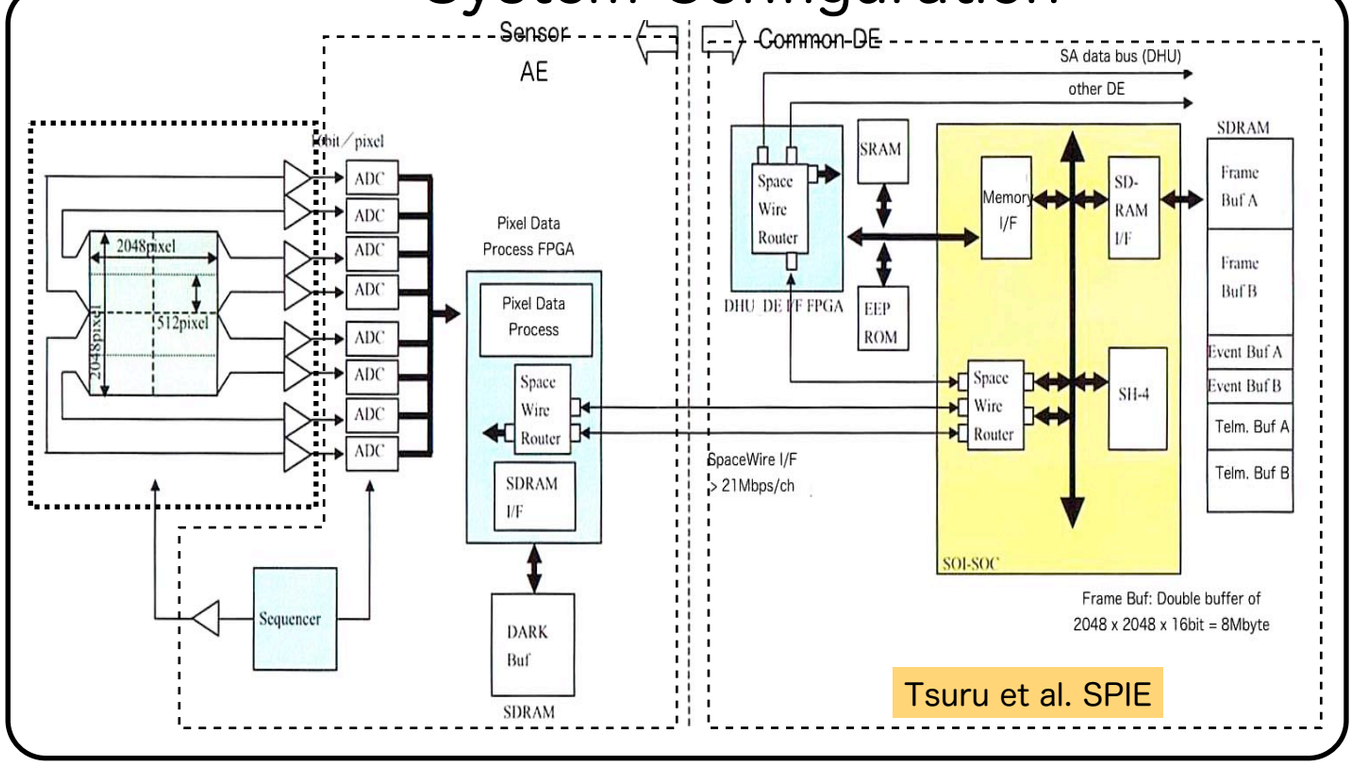
(Osaka Univ., Kyoto Univ., ISAS/JAXA, Rikkyo Univ., Ehime Univ., Kogakuin Univ.)

SXI is an X-ray CCD camera placed at the focal plane of Soft X-ray Telescopes for Imaging (SXT-I) onboard NeXT. The pixel size and the format of the imaging area of the CCD are 24μm×24μm and 2048×2048, respectively. We have been developing two types of CCD as candidates for SXI, in parallel. The one is front illumination type CCD with moderate thickness of the depletion layer (70～100μm) as a baseline plan. The other one is the goal plan, in which we develop back illumination type CCD with a thick depletion layer (200～300μm). For the baseline plan, we successfully developed the proto-model 'CCD-NeXT1' with the pixel size of 12μm×12μm and the CCD size of 24mm×24mm in the imaging area. The goal plan is realized by introduction of a new type of CCD 'P-channel CCD', which collects holes in stead of electrons in the common 'N-channel CCD'. By processing a test model of P-channel CCD we have confirmed high quantum efficiency above 10 keV with an equivalent depletion layer of 300μm. A back illumination type of P-channel CCD with a depletion layer of 200μm with aluminum coating for optical blocking has been also successfully developed. We have been also developing a thermoelectric cooler (TEC) with the function of the mechanically support of the CCD wafer without standoff insulators, for the purpose of the reduction of thermal input to the CCD through the standoff insulators. We have been considering the sensor housing and the onboard electronics for the CCD clocking, readout and digital processing of the frame date. The detail of the development is found in Tsuru et al. 2006 (SPIE).

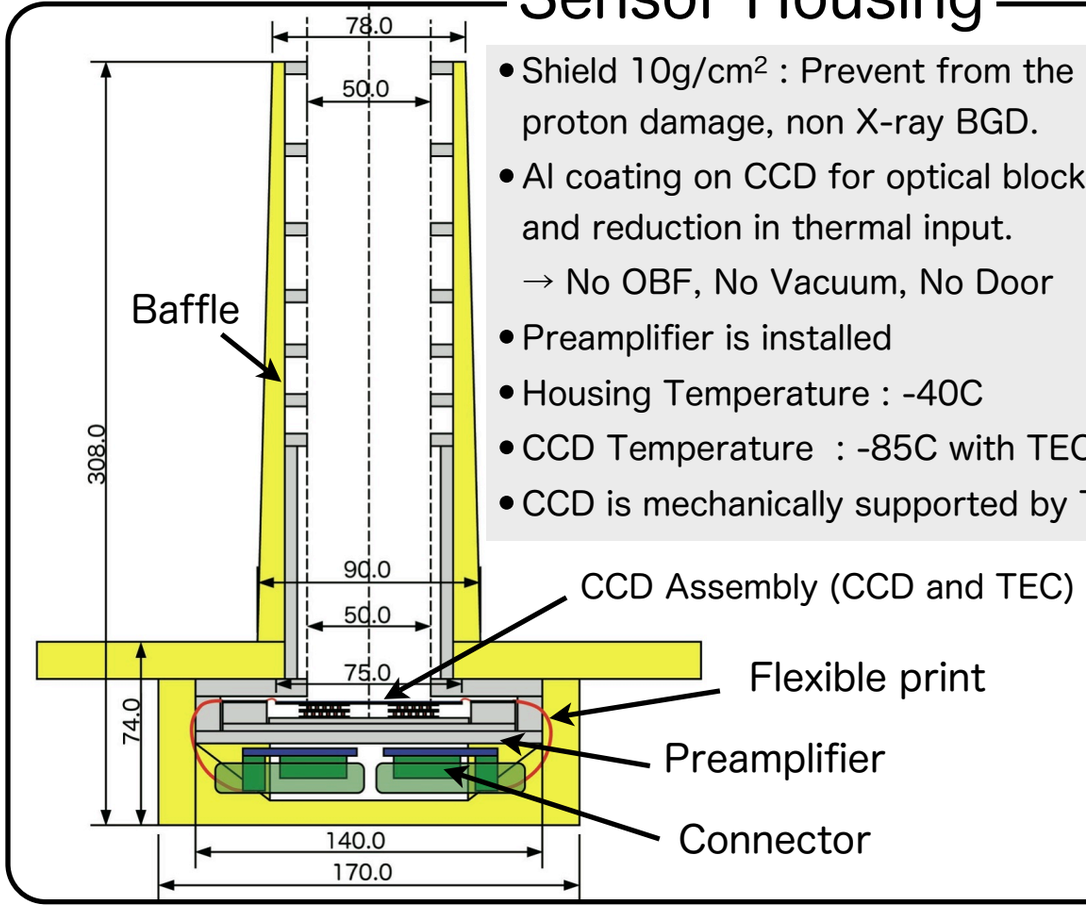
Specification of the CCD



System Configuration



Sensor Housing



- Shield 10g/cm² : Prevent from the proton damage, non X-ray BGD.
- Al coating on CCD for optical blocking and reduction in thermal input.
  → No OBF, No Vacuum, No Door
- Preamplifier is installed
- Housing Temperature : -40C
- CCD Temperature : -85C with TEC
- CCD is mechanically supported by TEC

Designing DE/AE

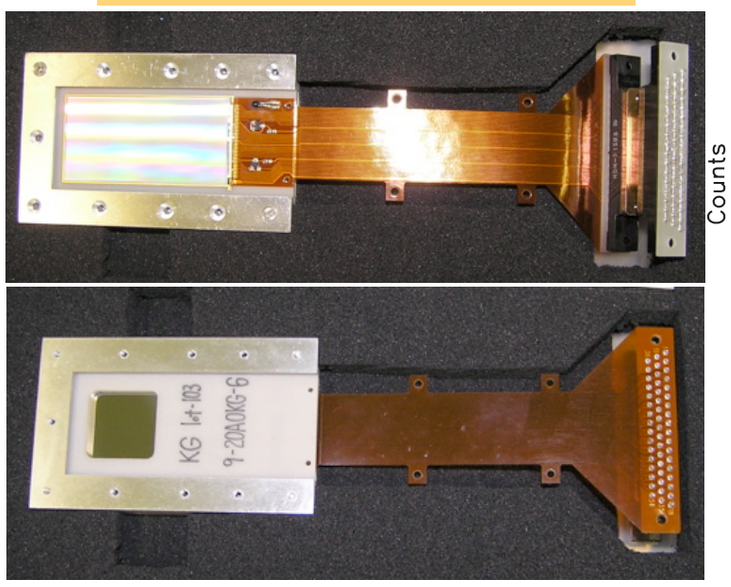
- Readout Cycle 4 sec (determined by anti-pile-up condition)
- High speed CCD clocking impacts the readout noise.
  - Equip 8 read out nodes in order to keep 131 kHz.
- CPU capacity of XIS-DE
  - Almost all the CPU time is used for the dark level subtraction of each pixel, which is proportional to the total pixel read out rate of the whole CCD.
  - SXI (1Mpix/sec) = 2 x XIS (0.5Mpix/sec)
- Common DE (Space Cube for NeXT)
  - 100-200MIPS = (2-4) x XIS-DE
  - Bench mark: Not impossible, but rather small margin.
  - Option: the hardwire event extraction with FPGA

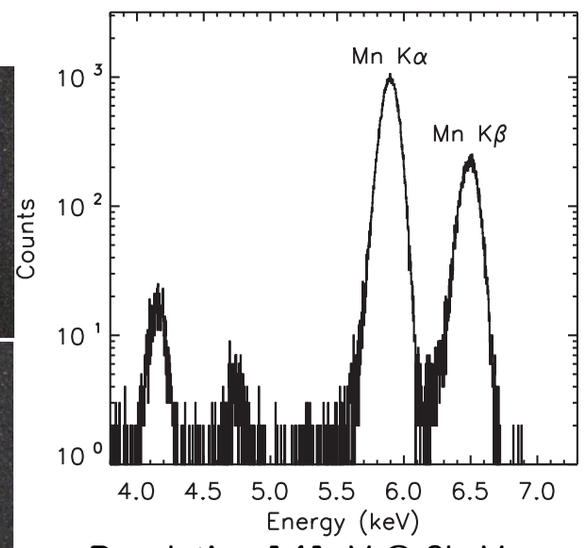
Ozaki et al. (2001), Anabuki et al. (2002)

- SpaceWire I/F (>21Mbps/ch)

N-ch CCD : CCD-NeXT1

Ozawa et al. SPIE. This Conf.



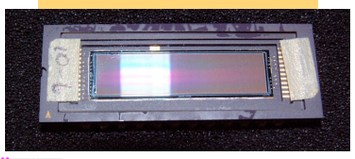


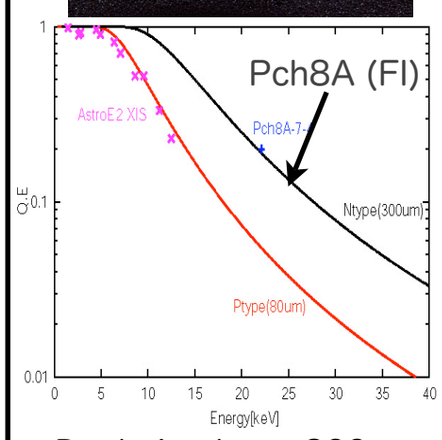
Resolution 141eV @ 6keV
Read Out Noise = 5e- (RMS)

- FI, depletion: 75-85μm + field free: 65-75μm
- 24 x 24mm² x 2 (IA + FS), pixel size 12 x 12um²
- Back Supportless (according to the original WXI)

P-ch CCD Test Device

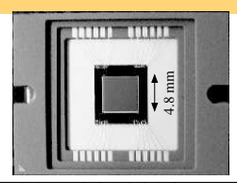
Takagi et al. NIM (2005)

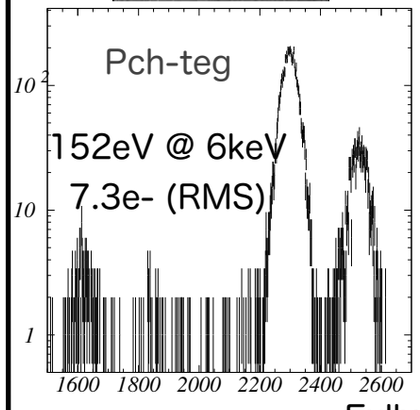




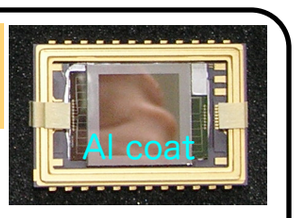
Deplation layer 300μm

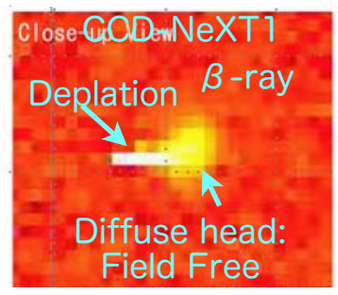
Matsuura et al. SPIE, This Conf.

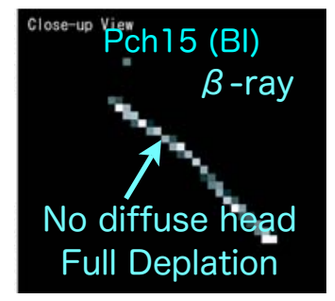




Takagi et al. SPIE, Thic Conf







Fully depleted BI 200μm,
Al coating 100nm