EURECA: Japanese Contributions and Status

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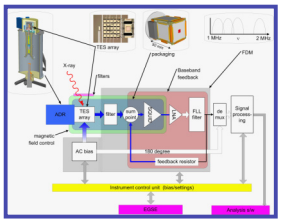
EURECA (EURopEan Carolimeter Array) project

5 x 5 TES array system as a proto-type of XEUS NFI, including 4 multiplexing readout channels, bias cuircuis, data acquisition system with de-multiplexing HW/SW, ADR dewar & control



Schematic of EURECA

TES array	SRON,MESA+
Entrance window	Leicester
SQUID/FLL	SRON,VTT,PTB, INAF, ISAS,TMU,SII
LC filter	INA/ICMA
Digital electronics	PSI &SRON
ADR	MSSL,INAF,PSI

Contributed institutes

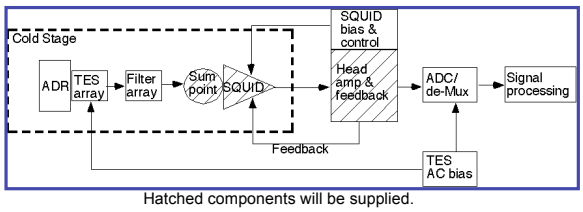
FDM readout channels

For multiplexing TES signals, we adopt Frequency-Domain Multiplexing (FDM). Still, there are several possibilities to be tried. EURECA will have 4 independent readout channels.

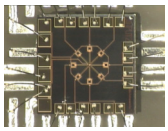
	Summing	SQUID	LNA	FLL	Developed by
1	Current-sum	SQUID array	Room-T	standard	PTB, SRON
2	Current-sum	2-stage SQUID	Room-T	baseband	VTT (PTB),SRON
3	Current-sum	SQUID array	Cold	standard	PTB,SRON, INFN?
4	Flux-sum	2-stage SQUID	Room-T	standard	ISAS, TMU, SII

Japanese channel

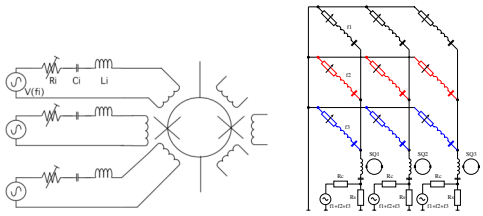
ISAS/TMU/SII team will provide analog circuits for "channel 4", which consists of flux-summation by 8-input SQUID with SQUID series array with Room-T standard Flux-Locked Loop (FLL) electronics.
Re-design to match bias frequencies, wiring and other characteristics in EURECA is underway.



Hatched components will be supplied.



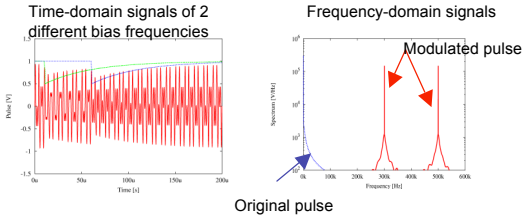
8-input SQUID developed by ISAS and SII.



Flux / current summation topologies.
Currents from TESs are read by SQUIDs.
Summing/feedback points are different.

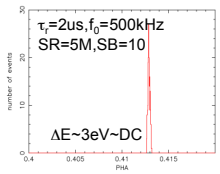
Current design parameters:
2-st SQUIDs:8-input SQUID with 80-SSA
Room-T FLL:Gain-BW product of 20 MHz
noise <2nV/√Hz

Digital de-MUX logic



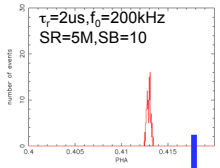
In FDM, TES signals are modulated by bias frequencies, and de-MUXed by FFT. A simulation to determine the requirements for pulse acquisition are carried.
For bias frequency < 2MHz, Sampling rate of 10MS and effective bits of 10 are required

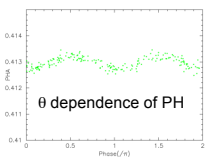
De-MUXed pulse height spectrum with noise equiv. to ΔE~3eV

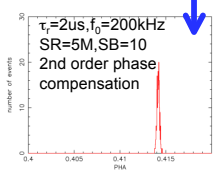


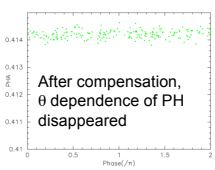
τ_r:Rise time of signal
f_0:Bias frequency
SR:Sampling rate
SB:Sampling bits
θ :Phase defined as
$f_{AC}(t)=f_{DC}(t)\cos(2\pi f_0 t+\theta)$

When $\tau_r f_0>1$, SR>$2f_0$ & SB >10 will be OK









When $\tau_r f_0<1$, θ-dependence of PH is observed.
Phase compensation for each pulse using θ determination and self-contradictious solution. This method needs SR>$4*2^n f_0$