NeXT SXI Data Processing System

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\textbf{ABSTRACT}

The Soft X-ray Imager (SXI) is the X-ray CCD detector system on board the NeXT mission that is to be launched around 2013. The system consists of a camera, an SXI-specific data processing unit (SXI-E) and a CPU unit commonly used throughout the NeXT satellite. All the analog signal handling is restricted within the camera unit, and all the I/O of the unit are digital.

The camera unit and SXI-E are connected by multiple LVDS lines, and SXI-E and the CPU unit will be connected by a SpaceWire (SpW) network. The network can connect SXI-E to multiple CPU units (the formal SXI CPU and neighbors) and all the CPU units in the network have connections to multiple neighbors: with this configuration, the SXI system can work even in the case that one SpW connection or the formal SXI CPU is down.

The main tasks of SXI-E are to generate the CCD driving pattern, the acquisition of the image data stream and HK data supplied by the camera and transfer them to the CPU unit with the Remote Memory Access Protocol (RMAP) over SpW. In addition to them, SXI-E also detects the pixels whose values are higher than the event threshold and both adjacent pixels in the same line, and send their coordinates to the CPU unit. The CPU unit can reduce its load significantly with this information because it gets rid of the necessity to scan whole the image to detect X-ray events.

\textbf{Keywords:} CCD, SpaceWire, SXI, NeXT

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1. INTRODUCTION

NeXT is the 6th Japanese X-ray astronomy satellite proposed to be launched in 2013\(^7\). The satellite aims to study the non-thermal processes in the Universe by observing X- and gamma-rays coming from many kinds of celestial bodies such as stars, interstellar plasma, black holes and gamma-ray bursts. For this purpose, NeXT has four types of detectors (SGD, SXS, HXI and SXI), and they all have different area of strength i.e., soft gamma-ray imaging, high energy resolution, hard and soft X-ray imaging spectroscopy, respectively.

The NeXT team chose to introduce a set of common data processing architecture consisting of the SpaceWire (SpW) network and the SpaceCube processing unit\(^7\) (Figure 1), in order to realize the satellite of such complicated functions with limited budget and resources and tight schedule. All the data processing components—not only the spacecraft controlling part but also payload instruments—will conform to this architecture, and it is expected that the test procedure during the satellite construction, which requires significant fraction of the construction schedule, becomes much simpler and shorter than previous JAXA spacecrafts.

SXI, the Soft X-ray Imager, is the CCD camera system sensitive to 0.2–20 keV X-rays\(^7\) which is similar to previous systems such as XIS\(^7\) onboard Suzaku\(^7\) or SIS onboard ASCA\(^7\). The system has one camera body including a $2 \times 2$ CCD array as the focal plane detector. Each CCD chip has $1280 \times 1280$ imaging pixels and two readout nodes, and the readout speed is about 200 kHz: thus, the exposure cycle of full-imaging mode becomes 4 sec. In the standard observation mode, the SXI system extracts X-ray events from each exposure frame and outputs their list consisting of the pixel levels and the time information as the telemetry.

In contrast to the previous Japanese X-ray astronomy satellites, all the electrical lines among the SXI components handle no analog signals: the CCD-driving signals are generated inside the camera body based on the configuration and the clock patterns supplied as digital signals from outside, and the outputs from the chip are digitized by the ASICs in the body and only digital outputs appear to the outside\(^7\). With this configuration, the SXI system consists of only universal equipments such as SpaceCube or field-programmable intelligent I/O unit with SpW interface except for the camera body and the temperature control system.

This paper describes the requirements and the goal design of the SXI data processing system. The development status of the bread board model (BBM) is also reported.
2. REQUIREMENTS AND GOAL DESIGN

The function of the SXI data processing system has three blocks: CCD driving, data acquisition (DAQ) and interface to the satellite's data handler. Figure 2 shows a schematic block diagram of the goal design of the SXI data processing system described below.

The CCD-driving part generates all the CCD-related timings and information such as the clock pattern, ADC trigger, pixel attribute information supplied to the DAQ part. The component in charge of those tasks is called Sequencer. The driving part also controls the DACs that set the high and low voltages of the chip driving and bias lines and collecting the HK information with commanding appropriate ADCs. The DAC-set and ADC-control actions are controlled or inhibit by Sequencer.

The DAQ part collects the digitized CCD outputs and sends them to the telemetry generation part as well as it updates the dark-level image, subtracts the dark level from the CCD outputs and extracts the X-ray-grade events. As the digitized CCD outputs require the decimation filter as a part of ΔΣ ADC at the each beginning of the data chain. The decimation filter's output is sent to the next stage only if the pixel attribute information supplied from Sequencer shows that the datum is of a valid pixel. In nominal operation, the outputs are stored as a “Frame image” after pixel-by-pixel dark-level subtraction. The dark level for each pixel has been calculated from the previous frame's dark and dark-subtracted pixel levels. In parallel to the frame accumulation, the pixel level is used to detect the event-center candidate whose value is higher than those of both neighbors and the event threshold. In contrast to the previous study, only the pixels in the same line will be used to detect a local peak candidate: thus additional peak detection process by software is essential for the real event extraction. The coordinates of the event-center candidates are stored as a “Event candidates”. The data stored as the Frame image and Event candidates are scanned by the “Event extraction” software, which reads out significantly reduced number of pixels from the Frame image by using the Event candidates’ information.

The data handler part sends out the telemetry as space packets recommended by CCSDS and receives command packets via SpW network. The telemetry packets are generated by the “Telemetry generation” part, which receives the outputs of the “Event extraction” software. For the diagnostic packets such as whole frame, raw frame or dark frame image or HK data, the “Telemetry generation” part reads out corresponding data directly.

To realize the design described above, we chose to divide the system into two parts: “SXI-DE”, which conforms to the SpaceCube architecture, and “SXI-E”, which contains a set of hardwired logic circuit highly specific to the SXI. Among those functions, the clock pattern generation should be implemented not by usual microprocessor but by DSPs or hardwired sequencer to control the clock timing precisely. Other components that are implemented as hardware include the dark-level calculation and subtraction and the event extraction. They would essentially require the units to scan all the input data and such scans need significant execution cycles if they are implemented as software running on a von Neumann-type computer.

In order to make SXI-E conform to the NeXT information architecture, we defined “Universal SpaceWire board” as the fundamental unit of SXI-E: SXI-E thus consists of one or multiple numbers of this board(s). Universal SpW board is characterized by a set of SpW interface, LVDS I/Os that can be used to communicate with non-SpW equipments, FPGAs and large memories connected to the FPGAs.

3. BBM DEVELOPMENT

As the BBM of the SXI processing system, we assigned two Universal SpW board BBMs whose features are shown below and a commercially-available SpaceCube as the platform for the three blocks introduced in the section 2, which can also be treated as loosely-connected components that can be developed independently. The schematic block diagram of the first-developed system is shown in Figure 3: this system drives a CCD chip with co-operating with the BBM of the analog part in the camera body, handles one node of the CCD outputs and stores the digitized values into the on-board memory without any dark-level subtraction. Two Universal SpW boards for the DAQ and Sequencer parts are called as “DE I/F board” and “Sequencer board”, respectively. The SXI-E BBM is defined as combination of those.

The Universal SpW board BBM consists of a pair of a FPGA (Xilinx XC3S400) and 32MB SDRAM, two SpW ports, 40 ch bidirectional LVDS ports and a parallel data channel that can be connected to other Universal
Figure 2. A schematic block diagram of the goal design of the SXI data processing system. The whole system consists of three major components: (1) the CCD driving block consisting of Sequencer, Driver-DAC controller, HK data collector and accompanying memories in SXI-E, (2) the DAQ block consisting of the modules and memories in 8-parallel rectangles of broken line and Pixel coordinate counter in SXI-E and the Event extraction and Telemetry generation modules as MPU tasks in SXI-DE (the data that MPU tasks require are transferred via SpW from other memories) and (3) the satellite interface block consisting of the Command handling MPU task and SpW middleware in SXI-DE that is invisible in this drawing.
Figure 3. A schematic block diagram of the first BBM design of the SXI data processing system. Many components such as Sequencer control via SpW, modules/tasks related to event extraction and the satellite interface were omitted because we gave priority to establishment of the data stream chain starting from Sequencer to SXI-DE through the SXI camera BBM.
SpW board directly. The data channel contains not only a parallel data bus but also several universal lines that can be used to exchange signals such as the pixel attribute information issued by Sequencer between two boards with arbitrary timing. Figure 4 shows a schematic block diagram of the Universal SpW board BBM.

3.1 DETAIL OF THE BBM COMPONENTS

Among the functions of the goal design, the first BBM includes the following components: preliminary Sequencer, the decimation filter coupled with the front-end ΔΣ-ADC ASIC design, the pixel attribute information handling between Sequencer and the acquisition control gate after the decimation filter, frame-data storing and communication with Remote Memory Access Protocol (RMAP) over SpW.

The currently implemented Sequencer is different from the goal design in the following points: the present one cannot be controlled from the outside of the module and begins running when the power of the BBM is activated, and the clocking pattern and the ADC values supplied to the analog driver stage are hardcoded in the source VHDL and unchangeable at the runtime. These are mainly because most of the interboard communication logic on the Sequencer board has not been implemented yet.

While the interboard communication logic has not been implemented yet, the pixel attribute information issued by Sequencer is supplied to the DE I/F board because its handling mechanism requires no address assignment or handshake. Consequently, the acquired data filtering based on the pixel attribute code (PCODE) is already implemented and working. Before the filtering gate, the offset value that is set via SpW is added to the digitized value.

The decimation filter in the DE I/F board was ported from a previously-developed IP used to test the ASIC and its test board: because this part is essential for the ADC to get a digitized value, the function of the IP had already been confirmed by many tests. The portation proceeded with no serious error, while not the VHDL source codes but the interface control document summarized from the design parameters and the past experimental results were transferred from Osaka-University to Mitsubishi Heavy Industry, Ltd. (MHI), which developed the ASIC and the BBM decimation filter, respectively.

While it is not stated explicitly in section 2, the function that stores and sends out the acquired data with no data reduction (i.e., raw-image data) is required as a basic equipment diagnostic method. The BBM has a function to accumulate the frame data that passed through the gate controlled by the PCODE from Sequencer into the on-board memory bank.

The on-board memory bank is transparently accessible by RMAP/SpW from SXI-DE and other SpW instruments. In addition to the memory, all the resources on the board are mapped on the RMAP memory space.
To realize that, we implemented RMAP function on the FPGA that is connected to the SpW physical interface and a 32-bit data bus among two FPGAs and the buffer chips for the interboard communication on the DE I/F board. The Frame data transfer from SXI-E to SXI-DE is realized with no additional mechanism, consequently.

While those functions have already been implemented, there remain many unimplemented features: the Dark image generation/update component, the event-candidate detection on the DE I/F board, the intraboard memory bus on the Sequencer board and HK data collector.

4. DISCUSSION

We performed the first BBM tests combining with the analog frontend BBMs of the SXI camera body. The schematic configuration with all the BBMs’ photographs is shown in Figure 5.

We confirmed the following features:

• Sequencer controls and drives the CCD-driving analog circuit BBM with proper pixel rate, and the DE I/F board acquires corresponding data. This means that Universal SpW board architecture is usable as the SXI-E components.

• The decimation filter output are filtered based on the PCODE supplied from Sequencer. This is the first step of the interboard communication of Universal SpW boards.

• We succeeded in obtaining an image data from the DE I/F board by the SpaceCube with RMAP.

These mean that the data stream chain starting from Sequencer to SXI-DE through the SXI camera BBM is established: this is the first important progress to implement the SXI system with conforming to the NeXT information system’s architecture. On the other hand, the following performances required explicitly or implicitly have not been archived yet by the first BBM:

• The data transfer throughput from the DE I/F board to SpaceCube through the SpW has not been measured yet; however, current speed should be slower than the required one (26 Mbps, coming from 4 sets of 1280×1280 pixels of 16 bit data will be transferred in 4 sec), mainly due to the bottle neck in the SpaceCube currently used. This must be fixed by a new implementation of the SpW interface in SXI-DE.

• The memory handling scheme of the Raw image (and the Frame image in future) has not been defined or implemented yet: SXI-E must send out one of the image to SXI-DE concurrently with storing the new images coming from the sensor. To realize this, a memory handling technique such as double buffer and its access procedure should be defined.

The present BBM acquires the data stream from only one readout node and no scalability is considered in the design, while the flight model has to handle 8 nodes simultaneously. From the practical point of view, the latent problems are not only the circuit scale but also the thickness of the wire harnesses; thus multiplexing mechanisms between the ADC outputs and the decimator inputs may be required. This is worth considering because the typical data rate of an ADC output is $10^2$ times of the pixel rate (i.e., $\approx 20$ Mbps) and a typical LVDS line can handle over 100 Mbps signal. The same thing should be considered for the CCD-driving lines, as well.

As initially planned, the BBM development was carried out at three sites simultaneously: Sequencer board and a prototype of the ADC-related interface at Osaka University, Universal SpW boards and its fundamental logics such as intraboard memory bus and SpW interface by MHI and the DAQ over SpW by JAXA-RIKEN-Kogakuin-Rikkyo group. While the MHI part is the base of all other works and usually expected to be built in advance of others, the concurrent development progressed quite well. This is because all other works are to produce logic or software products and the interface required by them such as the FPGA pin assignment or the RMAP memory address assignment were defined first. Some later-introduced changes such as the change of the FPGA pin assignment were well handled by using the pin definition file used for the VHDL design. This case implies that an FPGA board with high-level external interface such as RMAP/SpW is a good platform for quick product development.
5. SUMMARY

We designed the NeXT SXI data processing architecture conforming to the NeXT information architecture: the system consists of a SpaceWire (SpW) CPU unit (SpaceCube) and the SXI-specific logic circuits on Universal SpW boards with functions of SpW communication, field programmable logic, interboard communication and LVDS I/O ports that can communicate with the SXI camera body circuits. They are called as SXI-DE and SXI-E, respectively.

The BBM of the system does not have the full function yet; however, this succeeded in driving a CCD chip and acquiring the outputs from one of its readout node co-operating with the BBM boards of the camera body, selecting the necessary data, storing them in the memory unit onboard a Universal SpW board and acquiring the memory data by the SpaceCube.

Several important functions such as multi-node readout, event extraction and streaming readout via SpW have not been implemented or tested yet and they are subject to be developed in near future.

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REFERENCES

Figure 5. Photographs of all the BBM components including the analog parts that drive and read out the CCD chip. The arrows show the data flow among the circuit boards and the SpaceCube.